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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,602	03/30/2001	Joseph Jeddalah	MIC-4	6053

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EXAMINER

CHEN, TSE W

ART UNIT PAPER NUMBER

2116

DATE MAILED: 12/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/823,602	Applicant(s) JEDDELOH, JOSEPH	
	Examiner Tse Chen	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 October 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-41 and 43-53 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-41 and 43-53 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3, 9, 13-15, 21, 25-26, 29, 31-32, 38, 43-45, 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens et al., US Patent 6226729, hereinafter Stevens, in view of Hartwell, US Patent 6724850.

3. In re claim 1, Stevens discloses a method of selecting an operating speed [channel frequency] of a memory module interface [interfaces 530, 540, 544] in a computer system [fig.5], said system comprising a central processing unit [processor 595], a memory controller [MCH 500], and a plurality of memory modules [560, 565, 570], each memory module comprising a serial presence detect memory [572] [col.11, l.66 – col.12, l.14], said method comprising:

- Counting the number of said memory modules [fig.8a, 850; col.12, ll.62-67; table 4].
- Keeping a running tally [rim count] of the number of said memory modules based on said counting [850].
- Generating a clock signal at a frequency to provide an operating speed of said memory module interface [col.13, ll.41-49].
- Based on at least a final tally of the number of said memory modules, selecting only one clock signal to provide an operating speed [channel frequency] of said memory module

interface [col.13, ll.41-45; frequency selected based on final tally of every memory modules that are operable with frequency – i.e., selected frequency is to be operable with final tally of memory modules].

- In response to said selecting, providing said selected clock signal to all of said memory modules [col.13, ll.41-49].

4. Stevens did not discuss details of generating the clock signal.

5. Hartwell discloses a method comprising simultaneously generating multiple clock signals at different frequencies [slow and fast] [col.2, l.52 – col.3, l.10].

6. It would have been obvious to one of ordinary skill in the art, having the teachings of Hartwell and Stevens before him at the time the invention was made, to incorporate the teachings of Hartwell with the system of Stevens as the simultaneously generating of multiple clock signals at different frequencies taught by Hartwell is well known and suitable for use in selecting an operating speed for the system of Stevens. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to generate different frequencies in typical data processing systems that require different clock speeds [Hartwell: col.1, l.56 – col.2, l.49; provide deterministic operations in Stevens].

7. As to claims 2 and 44, Stevens discloses, wherein said selecting comprises generating memory module interface signals comprising clock, address, and data signals at a frequency based on said final tally of the number of said memory module count and operating speed information of said memory modules [Stevens: col.11, l.35 – col.12, l.22; col.13, ll.41-56].

8. As to claims 3, 15, 32, 45, Stevens discloses, comprising obtaining information from said serial presence detect memory that includes at least one characteristic [e.g., frequency data] of

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said memory module, wherein said selecting comprises selecting only one of said multiple clock signals based on at least said final tally of the number of said memory modules and said characteristic [col.13, ll.41-49; frequency selected based on queried frequency that is operable with final tally of every memory modules].

9. In re claim 9, Stevens and Hartwell disclose each and every limitation of the claim as discussed above in reference to claims 1 and 3.

10. In re claims 13, 25, 31, 43, Stevens and Hartwell disclose each and every limitation of the claim as discussed above in reference to claim 1. Stevens and Hartwell disclose the method of operating the computer system; therefore, Stevens and Hartwell disclose the computer system and associated means. Stevens discloses wherein said memory controller:

- Accesses said serial presence detect memory [col.11, l.66 – col.12, l.14].
- Keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory [fig.8a, 850; col.12, ll.62-67; table 4].
- Selects one of the clock frequencies for driving said memory module interface based on at least a final tally of the number of said memory modules [col.13, ll.41-45].

11. As to claim 14, Stevens discloses that the central processing unit is a microprocessor [processor 595].

12. In re claims 21, 26, 29, 38, 51, Stevens and Hartwell disclose each and every limitation of the claim as discussed above in reference to claims 3 and 13. Hartwell discloses a computer system [data processing system 100] comprising at least two phase locked loops [PLL 1 and 3] to generate respective clock signals of different frequencies [slow and fast] [col.2, l.52 – col.3, l.10].

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13. Claims 4-5, 7-8, 10-12, 16-17, 19-20, 22-24, 27-28, 30, 33-34, 36-37, 39-41, 46-47, 49-50, 52-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens and Hartwell as applied to claims 3, 13, 21 above, and further in view of Johnson et al., US Patent 5577236, hereinafter Johnson.

14. Stevens and Hartwell disclose each and every limitation of the claim as discussed above. Stevens and Hartwell did not discuss the details [e.g., specific data] of selecting one of the operating speeds.

15. Johnson discloses a method comprising obtaining information from a serial presence detect memory [flash memory] that includes at least one characteristic [factors 2-4] of a memory module, wherein a selecting comprises selecting one of the clocks based on at least said final tally of the number of said memory modules [factor 1] and said characteristic [col.8, ll.33-45; col.9, ll.4-18].

16. As to claims 4, 11, 16, 22-23, 33, 40, 46, 52, Johnson discloses said characteristic comprises the number of components [memory circuits] in each said memory module [col.9, ll.9-10].

17. As to claims 5, 12, 17, 24, 30, 34, 39, 41, 47, 53, Johnson discloses said characteristic comprises a speed grade [sort] of said memory module [col.9, ll.17-18].

18. As to claims 7, 10, 19, 27, 36, 49, Johnson discloses said characteristic comprises a type of said memory module [col.8, ll.33-41].

19. As to claim 8, 20, 28, 37, 50, Johnson discloses said characteristic comprises a physical layout of signal connections between said memory controller and said memory module [col.9, ll.11-16].

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20. It would have been obvious to one of ordinary skill in the art, having the teachings of Johnson, Stevens and Hartwell before him at the time the invention was made, to modify the system taught by Stevens and Hartwell to include the explicit teachings of Johnson [i.e., relating to specific serial presence detect data to be retrieved], in order to obtain the system capable of obtaining information from a serial presence detect memory that includes at least one characteristic of a memory module, wherein a selecting comprises selecting one of the clocks based on at least said final tally of the number of said memory modules and the specific characteristic. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to accurately read data from a memory that may vary in numbers and other attributes [Johnson: col.2, 1.46 – col.3, 1.50].

21. Claims 6, 18, 35, 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens and Hartwell as applied to claims 3, 13, 21 above, and further in view of Olarig et al., US Patent 6134638, hereinafter Olarig.

22. Stevens and Hartwell disclose each and every limitation of the claim as discussed above. Stevens and Hartwell did not discuss the details [e.g., specific data] of selecting one of the operating speeds.

23. Olarig discloses a method comprising obtaining information from a serial presence detect memory that includes at least one characteristic of a memory module [114], wherein a selecting comprises selecting one of the clocks based on said characteristic, wherein said characteristic comprises a manufacturer of said memory module [table 1; col.10, 11.25-37].

24. It would have been obvious to one of ordinary skill in the art, having the teachings of Olarig, Stevens and Hartwell before him at the time the invention was made, to modify the

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system taught by Stevens and Hartwell to include the explicit teachings of Olarig [i.e., relating to specific serial presence detect data to be retrieved], in order to obtain the system capable of obtaining information from a serial presence detect memory that includes at least one characteristic of a memory module, wherein a selecting comprises selecting one of the clocks based on at least said final tally of the number of said memory modules and the specific characteristic of the manufacturer. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to determine the preferred clock frequency and timing characteristics of the memory module [Olarig: col.10, ll.25-37].

Response to Arguments

25. Applicant's arguments filed October 12, 2006 have been fully considered but they are not persuasive.

26. Applicant argues that Stevens does not disclose “selecting a clock signal ‘based on at least a final tally of the number of said memory modules’ ... only refers to selecting a clock frequency ‘at which all RIMMs may operate’”. Upon further review and reconsideration, Examiner disagrees and submits the following. As Applicant correctly pointed out, Stevens discloses selecting a clock frequency at which all RIMMs may operate [col.13, ll.44-45], by querying every RIMMs present. Without a final tally to be based upon, Stevens’ invention would not work because not every memory module would be operative with the selected clock signal [e.g., too fast]. Thus, Stevens discloses that the clock signal ultimately selected must be operable by the final tally of the number [i.e., all/every] of the memory modules.

27. Applicant argues that Stevens “does not select a faster clock signal when there are only two memory modules or a slower clock signal when there are four or more memory modules...

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selects a clock signal frequency that is compatible with all of the memory modules whatever the number of memory modules". Upon further reflection, Examiner disagrees and submits the following. Applicant's claims clearly stipulates that the selected clock signal is based on a *final tally* of the number of said memory modules which Stevens is shown to disclose as discussed above. In the scenario Applicant presented, Stevens does disclose selecting a faster clock signal when there is a final tally of only two memory modules or a slower clock signal when there is a final tally of four or more memory modules if the clock signal which the final tally of two memory modules are operable is faster than the clock signal which the final tally of four or more memory modules are operable [i.e., a slowest memory module is in the four or more memory modules group]. Examiner was not able to find enabling means in the original disclosure for Applicant's scenario where the selected clock signal when there are only two memory modules is faster than when there are four or more memory modules if the slowest memory module of either group exists when there are only two memory modules [i.e., group of memory modules operate at the clock signal of the weakest link].

28. As such, Applicant's arguments are deemed not persuasive and the rejections are respectfully maintained.

Conclusion

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after

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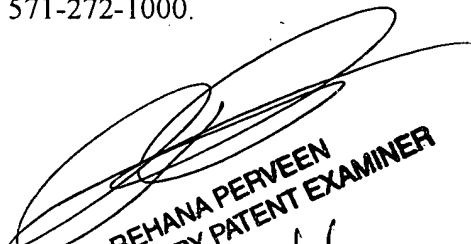
the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen
November 20, 2006


REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
11/29/06